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Title: PORTABLE COMPUTER HAVING DUAL CLOCK MODE

IN THE CLAIMS

1. (Previously Presented) A portable computer having a first power mode and a second power mode, comprising:

a first memory bus;

a second memory bus; and

a control system coupled to the first memory bus and the second memory bus, wherein the control system is configured to operate the first memory bus and the second memory bus at a first speed in the first power mode, and a second speed different than the first speed in the second power mode.

2. (Original) The computer of claim 1, where in the first power mode, the portable computer is operated via a battery power source, and in the second power mode the computer is operated via an external power source.

3. (Original) The computer of claim 1, further comprising a power mode detector which detects whether the portable computer is in the first power mode or the second power mode.

4. (Original) The computer of claim 1, wherein the control system includes the power mode detector.

5. (Original) The computer of claim 1, wherein the second bus speed is double the first bus speed.

6. (Original) The computer of claim 1, further comprising a clock generator coupled to the control system for generating a clock corresponding to the first bus speed and the second bus speed.

7. (Original) The computer of claim 1, further comprising a bus speed input for switching the portable computer between the first bus speed and the second bus speed.

8. (Original) The computer of claim 1, wherein the control system includes processor and a chipset.

9. (Original) The computer of claim 8, wherein the memory bus is in communication with the chipset.

10. (Original) The computer of claim 1, further comprising an override switch coupled to the control system for switching the memory bus to the first speed or the second speed.

11. (Previously Presented) A computer having a first battery power mode and a second external power mode, the computer comprising:

a random access memory;

a read only memory;

a first memory bus in communication with the random access memory;

a second memory bus in communication with the read only memory; and

a control system coupled to the first memory bus for reading and writing the random access memory and to the second memory bus for reading the read only memory, the control system including a clock generator, wherein the control system is configured to operate the first memory bus and the second memory bus at a first clock speed in the first battery power mode, and a second clock speed greater than the first clock speed in the second power mode.

12. (Original) The computer of claim 11, further comprising a power mode detector which provides an indicator to the control system as to whether the portable computer is in the first battery power mode or the second external power mode.

13. (Original) The computer of claim 11, wherein the second bus speed is double the first bus speed.

14. (Original) The computer of claim 12, further comprising a bus speed input for switching the portable computer between the first bus speed and the second bus speed.

15. (Original) The computer of claim 1, wherein the control system includes a processor and a chipset.

16. (Original) The computer of claim 8, wherein the memory bus is in communication with the chipset, and the chipset is in communication with the clock generator.

17. (Previously Presented) A mobile computing device having a first battery power mode and a second external power mode, the device comprising:

a random access memory;

a read only memory;

a first memory bus in communication with the random access memory;

a second memory bus in communication with the read only memory; and

a control system coupled to the first memory bus for reading and writing the random access memory and to the second memory bus for reading the read only memory, the control system including a clock generator, wherein the control system is configured to operate the first memory bus and the second memory bus at a first clock speed in the first battery power mode, and a second clock speed greater than the first clock speed in the second power mode.

18. (Original) The device of claim 17, wherein the mobile computing device is a laptop computer.

19. (Original) The device of claim 17, wherein the mobile computing device is a personal digital assistant.

20. (Original) The device of claim 17, wherein in the first battery power mode the device is coupled to an internal battery power supply, and in the second external power mode the device is coupled to an external battery power supply.

21. (Previously Presented) A method of managing power in a mobile computing device comprising:

determining whether the mobile computing device is operating in a first power mode or a second power mode;

operating a first memory bus and a second memory bus at a first bus speed when the mobile computing device is in the first power mode; and

operating the first memory bus and the second memory bus at a second bus speed different from the first bus speed when the mobile computing device is in the second power mode.

22. (Original) The method of claim 21, further comprising controlling a clock generator to determine the memory bus speed.

23. (Original) The method of claim 21, further comprising:
determining the memory bus speed independent of an internal processor bus speed.

24. (Original) The method of claim 21, further comprising:
defining the first power mode to be a battery power mode; and
defining the second power mode to be an external power source mode.

25-27. (Cancelled).

28. (Previously Presented) A mobile computing device having a first battery power mode and a second external power mode, the device comprising:

a random access memory;

a read only memory;

a first memory bus in communication with the random access memory;

a second memory bus in communication with the read only memory; and

a control system coupled to the first memory bus for reading and writing the random access memory and to the second memory bus for reading the read only memory;

a clock generator in communication with the control system, wherein the control system is configured to operate the first memory bus and the second memory bus at a first

clock speed in the first battery power mode, and a second clock speed in the second power mode; and

a performance level input in communication with the control system for defining the first clock speed and the second clock speed.

29. (Previously Presented) The device of claim 28, further comprising:

wherein the performance level input is configured to allow a user to select between a slow memory bus speed or a fast memory bus speed relative to the slow memory bus speed for the first clock speed and the second clock speed.

30. (Previously Presented) The device of claim 29, further comprising:

wherein the performance level input is configured to allow a user to select a user defined memory bus speed for the first clock speed and the second clock speed.

31. (Previously Presented) The device of claim 28, further comprising:

wherein the performance level input is configured to include a power mode over-ride setting for the first battery power mode and the second power mode, including allowing a user to select between a slow memory bus speed, a fast memory bus speed, or a user-defined memory bus speed.